ABSTRACT OF THE DISCLOSURE

A fail repair circuit of a nonvolatile ferroelectric memory device and a method for repairing the same are disclosed, in which a redundancy time can be reduced and a redundancy algorithm can be changed or added at any time. The fail repair circuit includes: a memory test logic block generating a redundancy active pulse (RAP) if a row address including a fail bit to be repaired is found during test; a power-up sensor generating a power-up pulse if a stable power source voltage is sensed; a first redundancy control block generating first to fifth control signals ENN, ENP, EQN, CPL, and PREC and a sixth control signal ENW in response to the RAP and the power-up pulse; a counter generating n bit counter bit signal increased by one bit through the RAP to correspond to the number of redundancy bits; a redundancy counter decoding control block generating an activated coding signal ENW<n> in response to the counter bit signal of the counter and the sixth control signal ENW; and a redundancy coding block outputting a master signal in response to the coding signal ENW<n> and the first to fifth control signals, programming a fail address in a plurality of redundancy coding cells, and outputting seventh and eighth control signals REN<n> and RPUL<n> to repair the programmed fail address.